FIG. 1

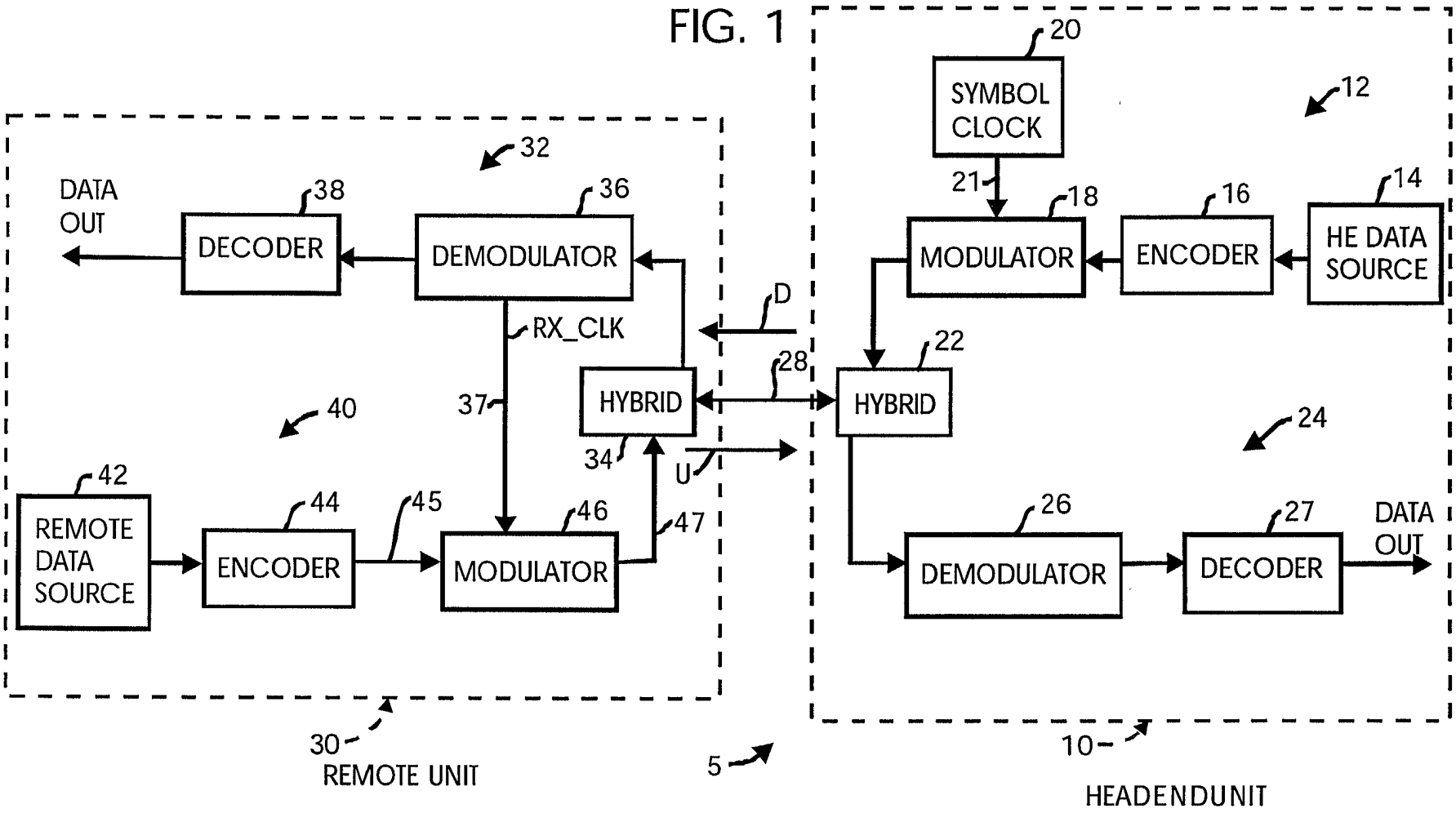

SYMBOL CLOCK
20
12
21
18
16
14
HE DATA SOURCE
ENCODER
MODULATOR
32
DATA OUT
38
36
DECODER
DEMODULATOR
D
RX_CLK
22
28
HYBRID
HYBRID
37
40
24
34
U
42
44
45
46
47
26
27
DATA OUT
REMOTE DATA SOURCE
ENCODER
MODULATOR
DEMODULATOR
DECODER
30
REMOTE UNIT
5
10
HEADENDUNIT

FIG. 2

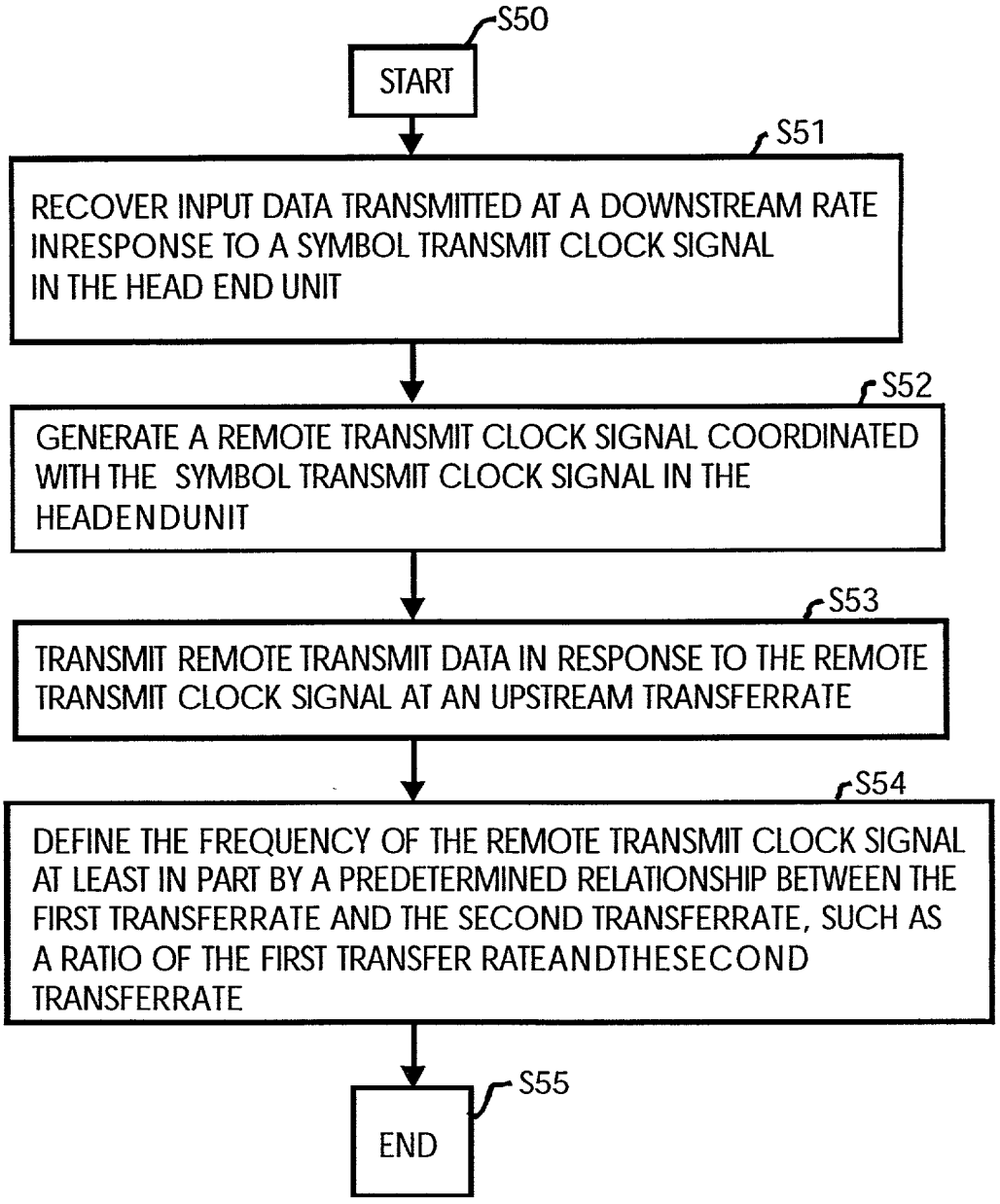

S50
START
S51
RECOVER INPUT DATA TRANSMITTED AT A DOWNSTREAM RATE INRESPONSE TO A SYMBOL TRANSMIT CLOCK SIGNAL IN THE HEAD END UNIT
S52
GENERATE A REMOTE TRANSMIT CLOCK SIGNAL COORDINATED WITH THE SYMBOL TRANSMIT CLOCK SIGNAL IN THE HEADENDUNIT
S53
TRANSMIT REMOTE TRANSMIT DATA IN RESPONSE TO THE REMOTE TRANSMIT CLOCK SIGNAL AT AN UPSTREAM TRANSFERRATE
S54
DEFINE THE FREQUENCY OF THE REMOTE TRANSMIT CLOCK SIGNAL AT LEAST IN PART BY A PREDETERMINED RELATIONSHIP BETWEEN THE FIRST TRANSFERRATE AND THE SECOND TRANSFERRATE, SUCH AS A RATIO OF THE FIRST TRANSFER RATEANDTHESECOND TRANSFERRATE
S55
END

FIG. 3

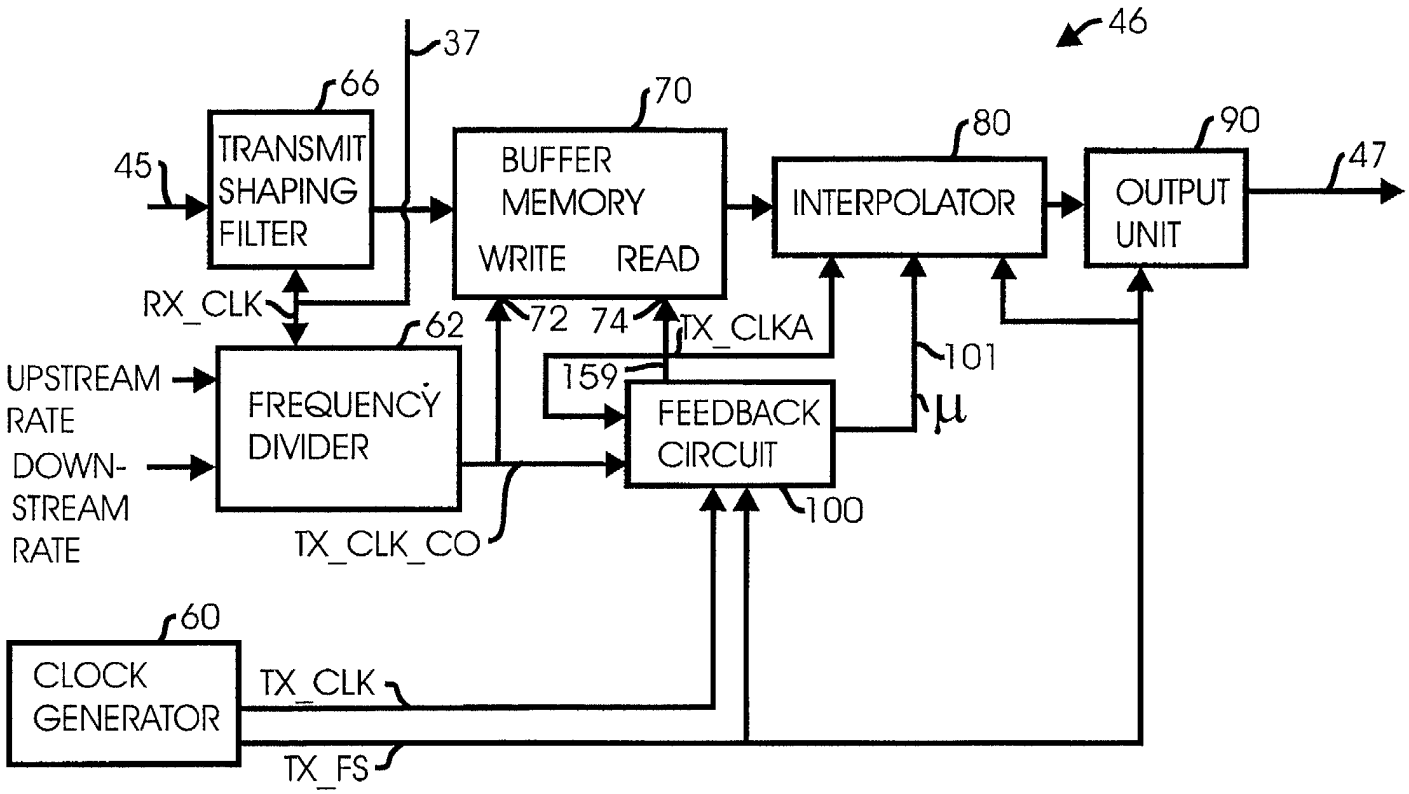

46
37
66
70
80
90
45
TRANSMIT SHAPING FILTER
BUFFER MEMORY
WRITE READ
INTERPOLATOR
OUTPUT UNIT
47
RX_CLK
62
72
74
TX_CLKA
101
159
UPSTREAM RATE
DOWN-STREAM RATE
FREQUENCY DIVIDER
FEEDBACK CIRCUIT
μ
100
TX_CLK_CO
60
CLOCK GENERATOR
TX_CLK
TX_FS

FIG. 4

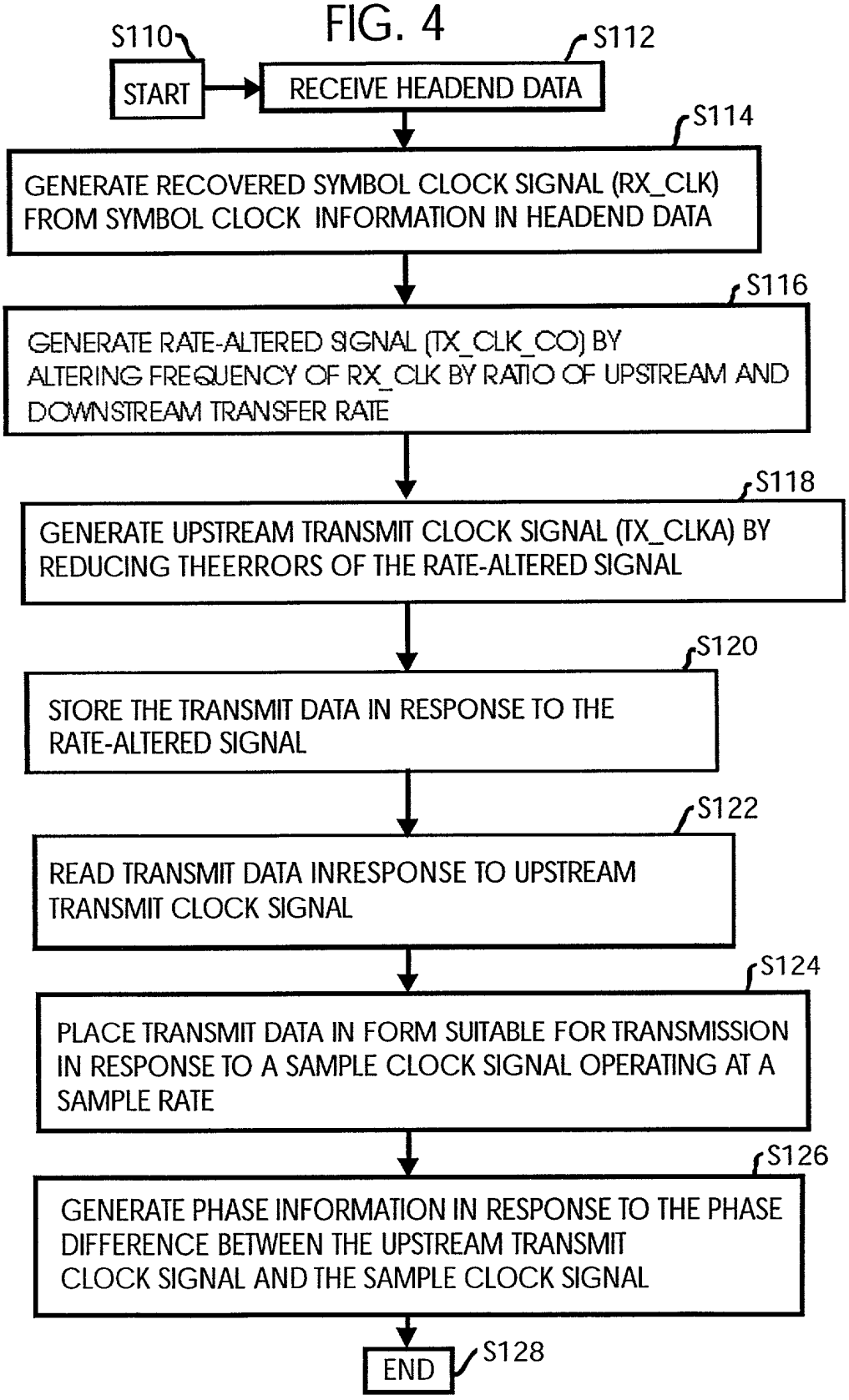
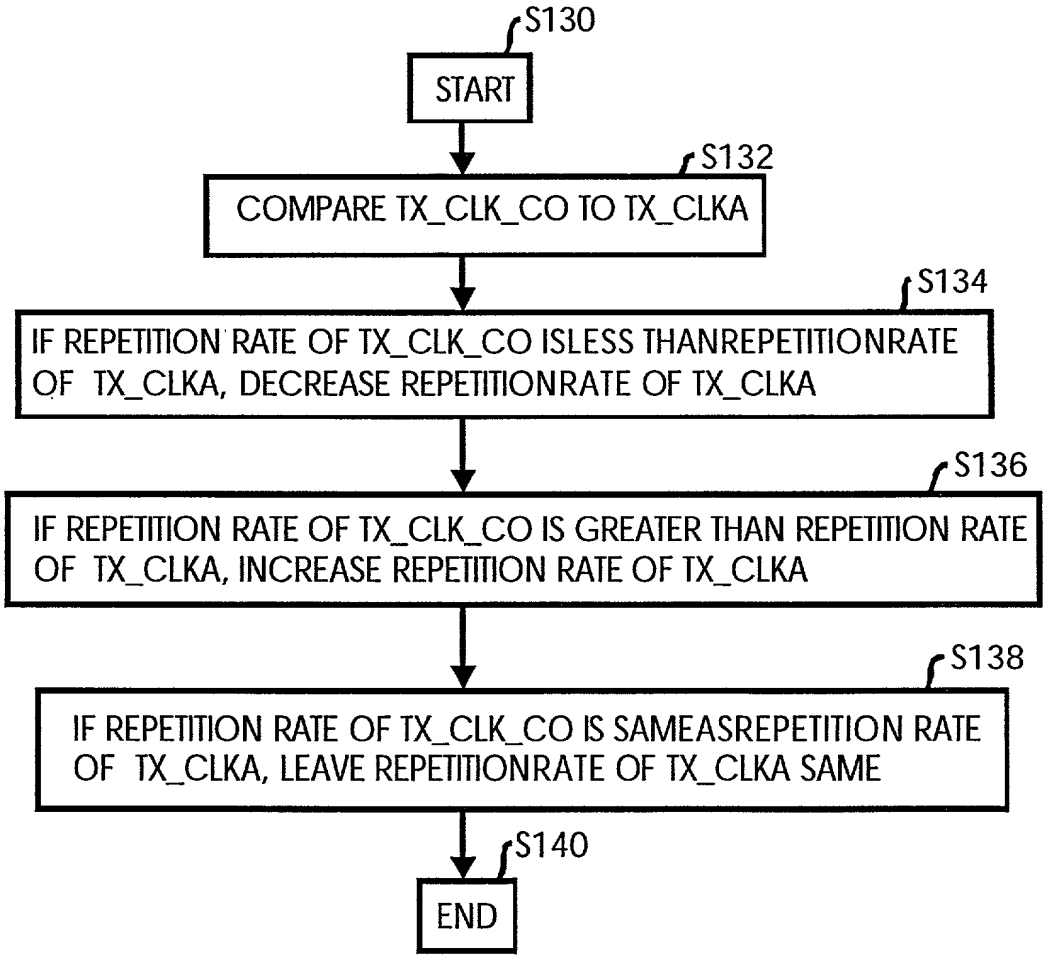

S110
START
S112
RECEIVE HEADEND DATA
S114
GENERATE RECOVERED SYMBOL CLOCK SIGNAL (RX_CLK) FROM SYMBOL CLOCK INFORMATION IN HEADEND DATA
S116
GENERATE RATE-ALTERED SIGNAL (TX_CLK_CO) BY ALTERING FREQUENCY OF RX_CLK BY RATIO OF UPSTREAM AND DOWNSTREAM TRANSFER RATE
S118
GENERATE UPSTREAM TRANSMIT CLOCK SIGNAL (TX_CLKA) BY REDUCING THEERRORS OF THE RATE-ALTERED SIGNAL
S120
STORE THE TRANSMIT DATA IN RESPONSE TO THE RATE-ALTERED SIGNAL
S122
READ TRANSMIT DATA INRESPONSE TO UPSTREAM TRANSMIT CLOCK SIGNAL
S124
PLACE TRANSMIT DATA IN FORM SUITABLE FOR TRANSMISSION IN RESPONSE TO A SAMPLE CLOCK SIGNAL OPERATING AT A SAMPLE RATE
S126
GENERATE PHASE INFORMATION IN RESPONSE TO THE PHASE DIFFERENCE BETWEEN THE UPSTREAM TRANSMIT CLOCK SIGNAL AND THE SAMPLE CLOCK SIGNAL
END
S128

FIG. 5


S130
START
S132
COMPARE TX_CLK_CO TO TX_CLKA
S134
IF REPETITION RATE OF TX_CLK_CO ISLESS THANREPETITIONRATE OF TX_CLKA, DECREASE REPETITIONRATE OF TX_CLKA
S136
IF REPETITION RATE OF TX_CLK_CO IS GREATER THAN REPETITION RATE OF TX_CLKA, INCREASE REPETITION RATE OF TX_CLKA
S138
IF REPETITION RATE OF TX_CLK_CO IS SAMEASREPETITION RATE OF TX_CLKA, LEAVE REPETITIONRATE OF TX_CLKA SAME
S140
END

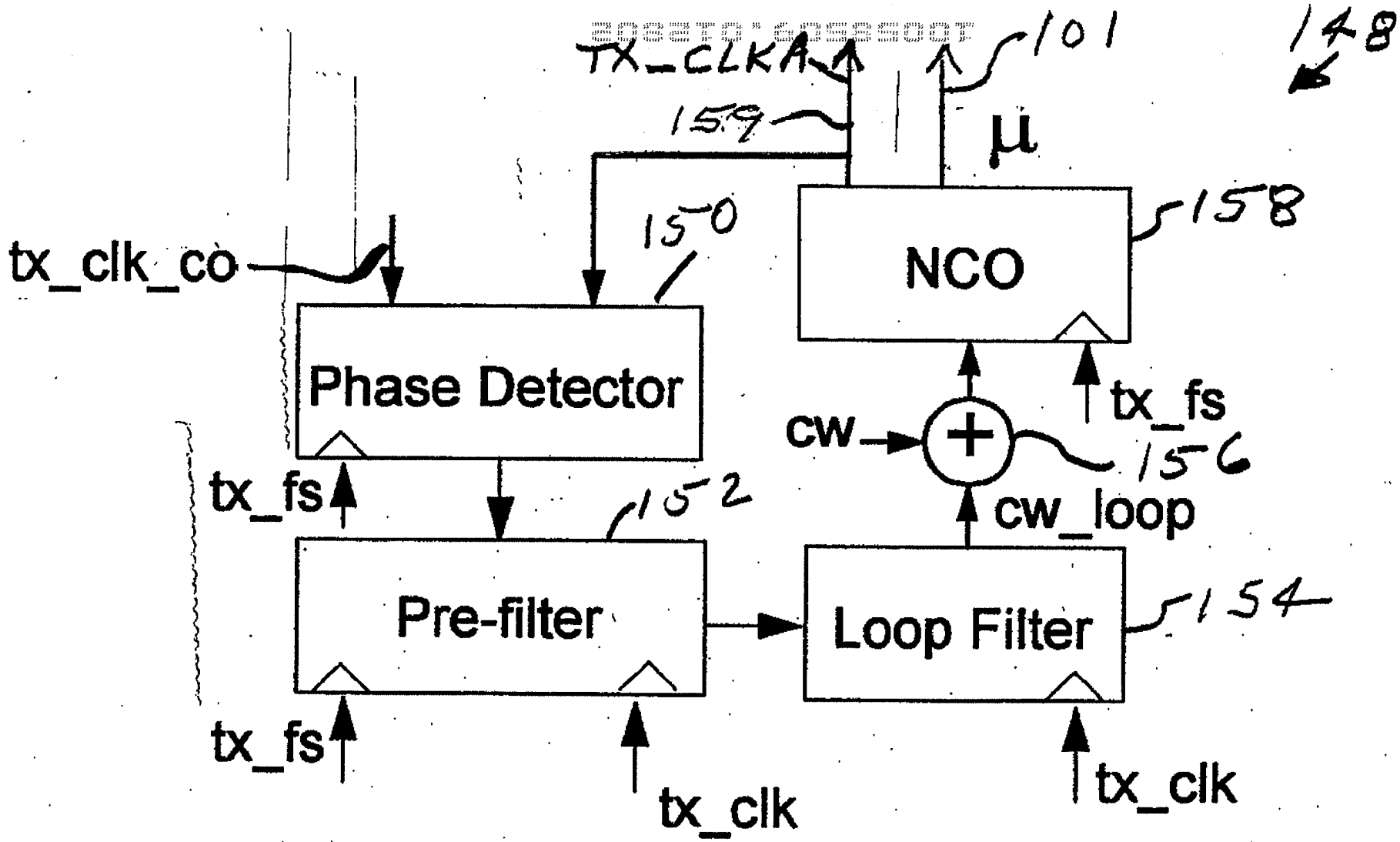

TX_CLKA
101
148
159
μ
150
158
tx_clk_co
NCO
Phase Detector
tx_fs
cw
156
tx_fs
152
cw_loop
Pre-filter
Loop Filter
154
tx_fs
tx_clk
tx_clk

FIG. 6

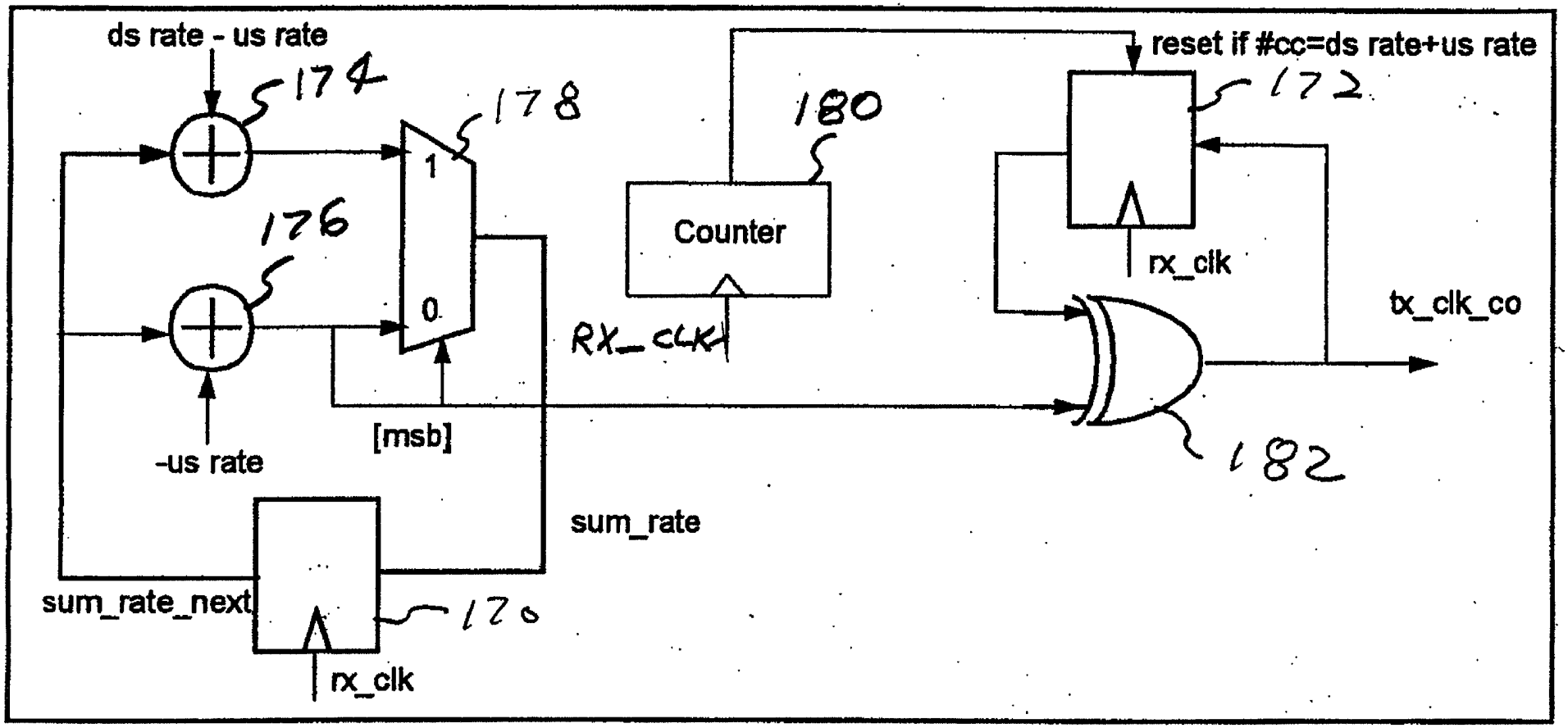


FIG. 7

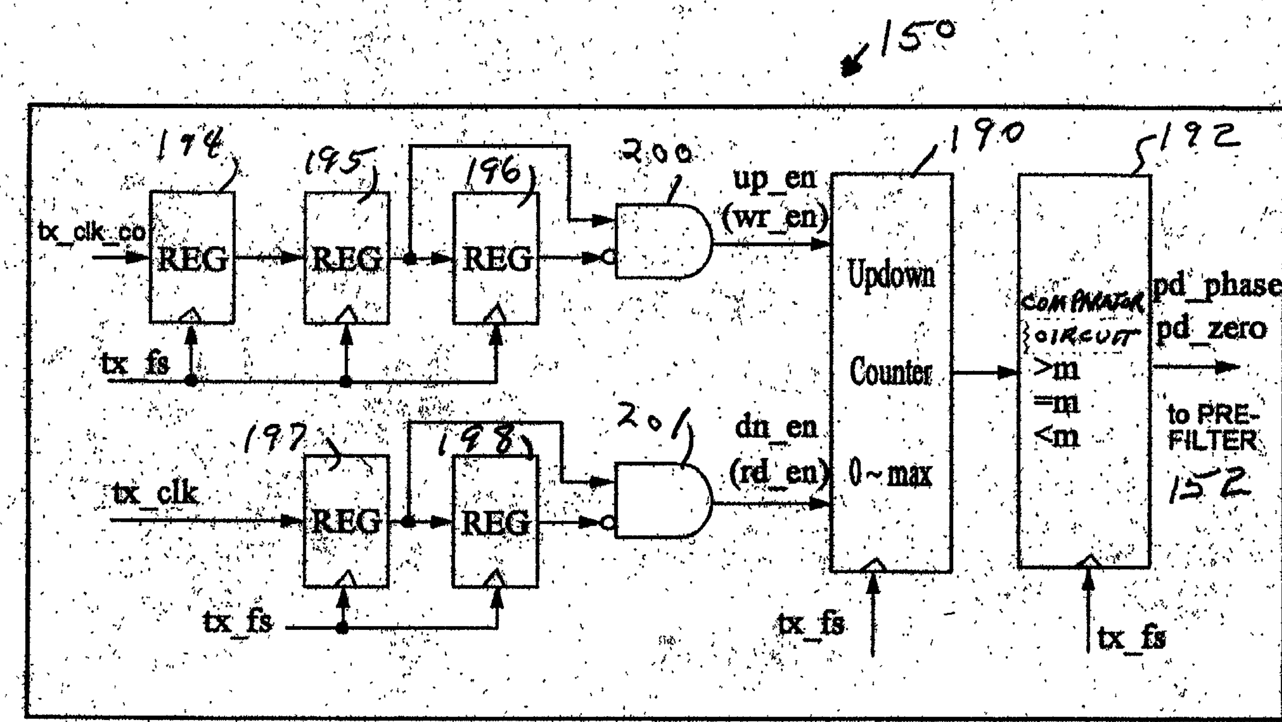

150
174
195
196
197
198
200
201
190
192
tx_clk_co
REG
REG
REG
tx_fs
tx_clk
REG
REG
tx_fs
up_en
(wr_en)
dn_en
(rd_en)
Updown
Counter
0~max
tx_fs
COMPARATOR
CIRCUIT
>m
=m
<m
tx_fs
pd_phase
pd_zero
to PRE-
FILTER
152

FIG. 8

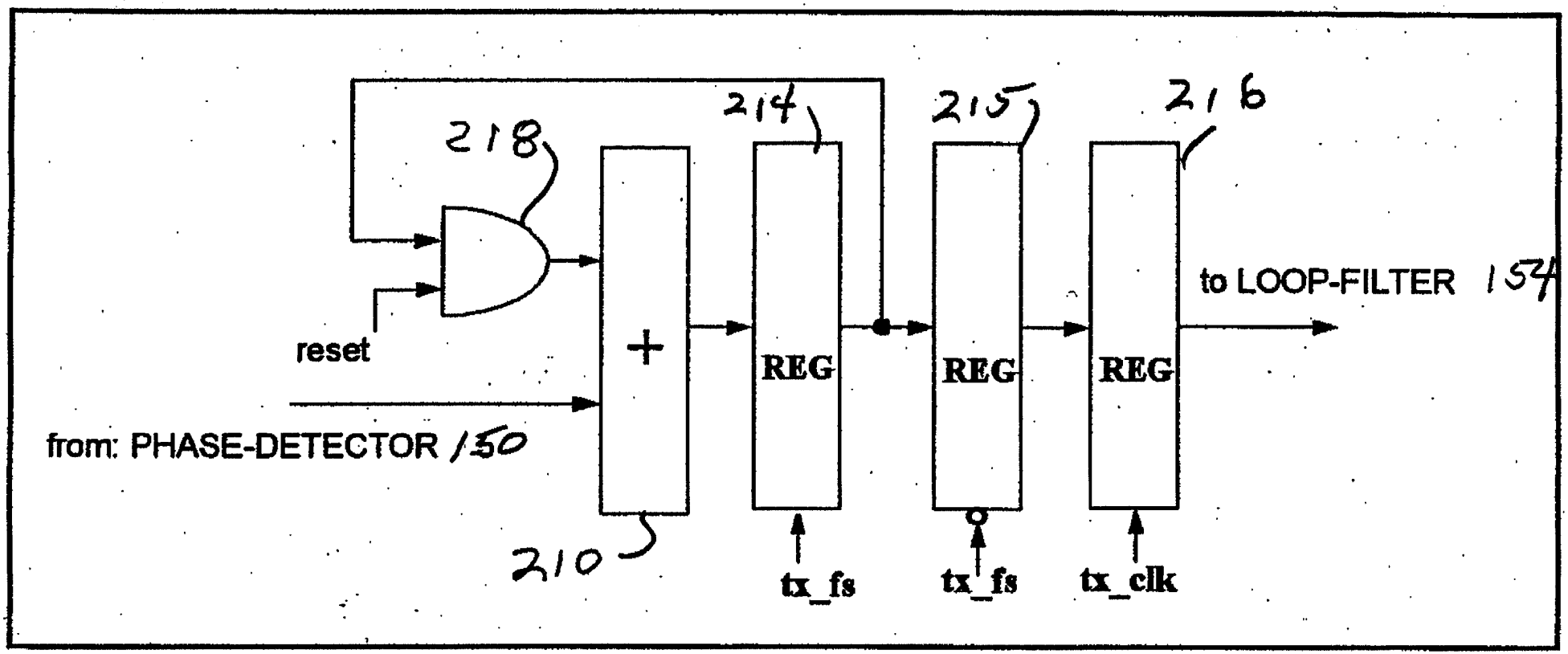


FIG. 9

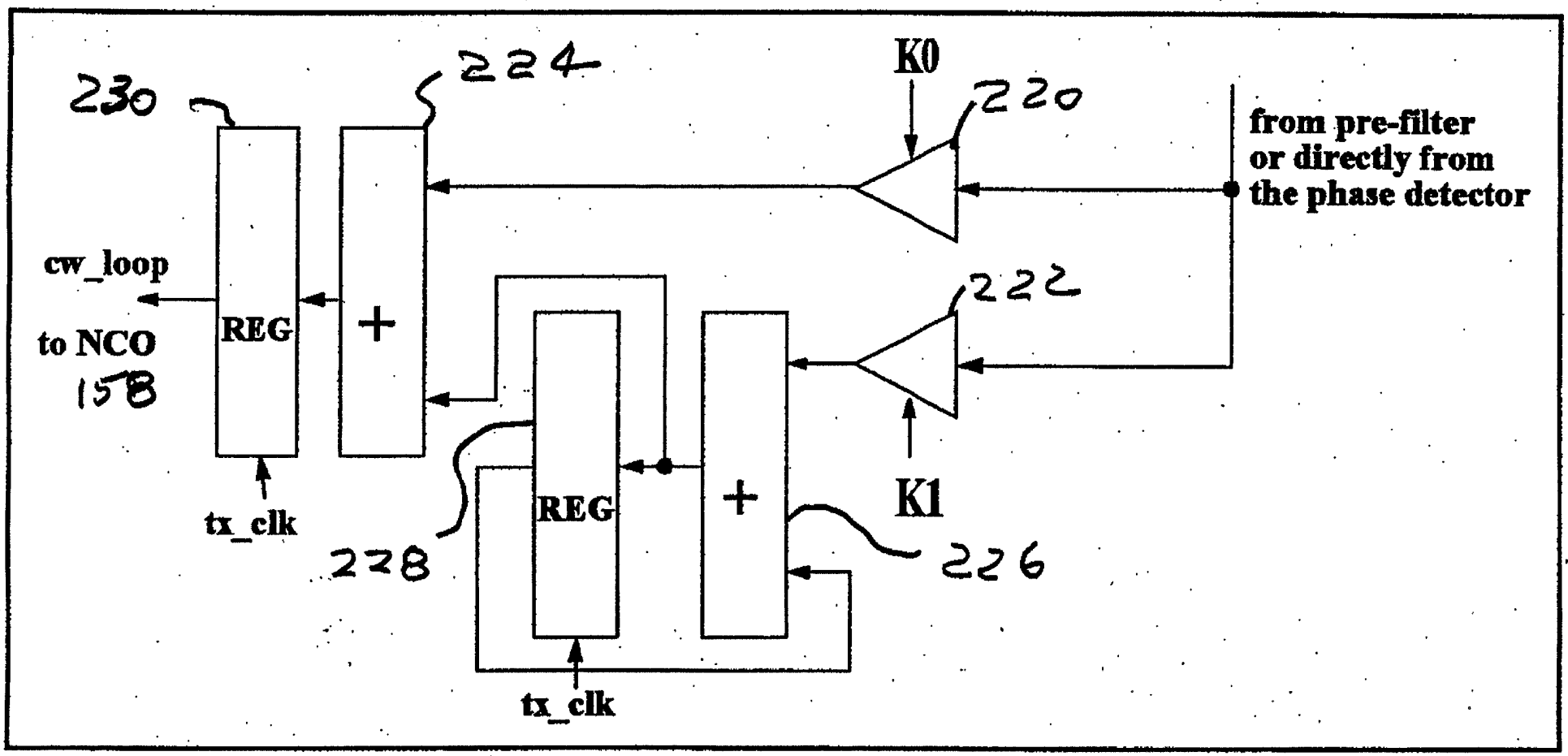

230
224
K0
220
from pre-filter
or directly from
the phase detector
cw_loop
to NCO
15B
REG
+
222
tx_clk
228
REG
+
K1
226
tx_clk

FIG. 10

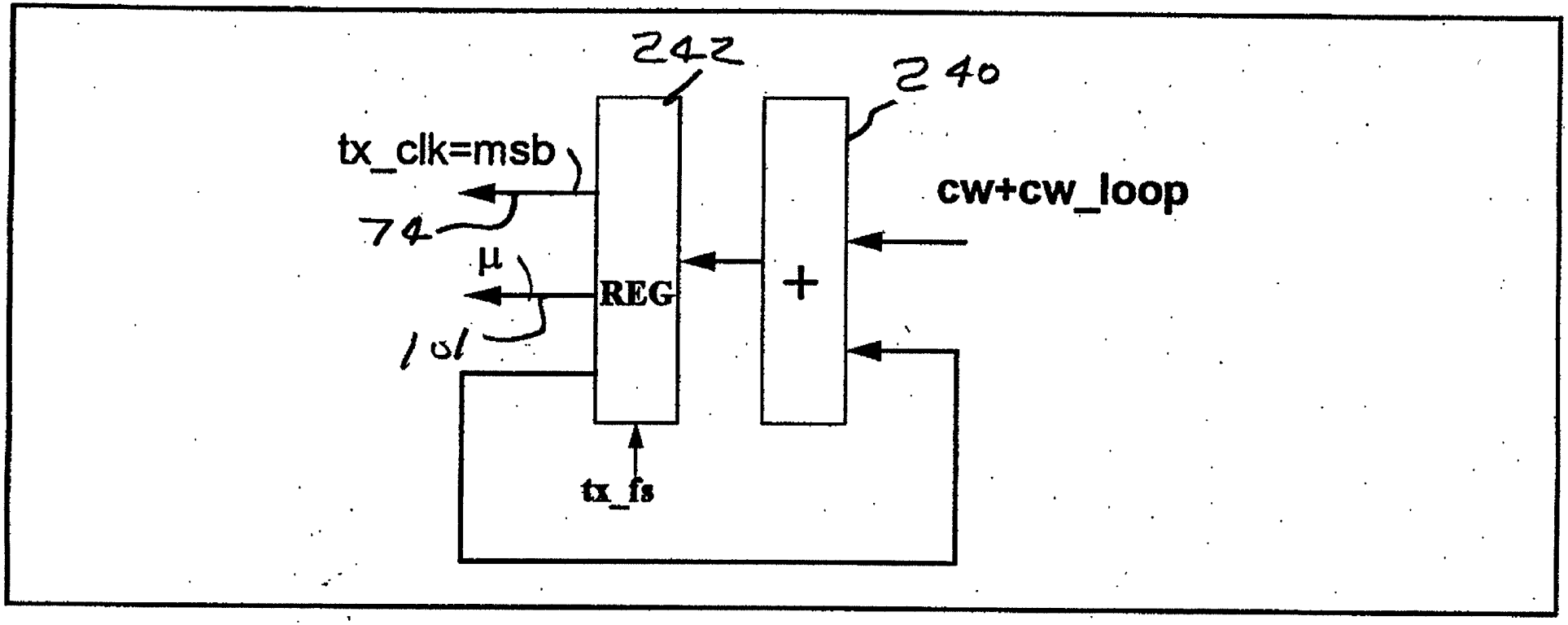


FIG. 11